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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	**PAPER NUMBER**
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/654,920	ENDO ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *14-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/09/2007 has been entered.

Response to Amendment

2. Amendment filed on 03/09/2007 has been entered.
In response to the Office Action dated 10/20/ 2006, Applicants have amended claim 1.
Claims 14-16 had been withdrawn from consideration.
Claims 1-16 are now pending in the application.

Response to Arguments

3.1. Applicant's arguments filed 01/12/2007 have been considered but are moot in view of the new grounds of rejection. Nevertheless, examiner points out, that applicant's arguments with respect to independent claim 1 are not persuasive. The Applicant discloses ".:. APA fails to cure the deficiencies of Okubora. APA merely teaches a multilayered wiring substrate including porous sheets. APA does not teach or suggest at least, "an electronic device directly connected to said wiring conductors located within the pores," as recited in independent claim 1 and required by dependent claims 2-4, 6, 8, and 9. However APA clearly teaches "a three-dimensional structure of the substrate including continuous pores " (JP-2001-083347, Abstract). And moreover, not only

Okubora, but and APA teaches "A structure of a package fabricated by the prior art flip chip bonding is illustrated in FIG. 1. For both or one of a semiconductor chip 1 and a wiring substrate 2, terminal electrodes 12 are prepared by forming bumps 4 of gold or solder material in advance", (Specification, page 1, lines 25-29). Applicant cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

3.2. Applicant's arguments with respect to dependent claims 2-12 are considered and acknowledged but they are not persuasive as based on arguments with respect to independent claim 1 as discussed above.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.1 Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Hotta et al. (PGPub. #2002/0004180) hereinafter Hotta. (Examiner's Note: Admitted by Applicant Prior Art (Background of Invention section and Fig. 1), hereinafter APA is used as evidence, as explained in the rejections below, in accordance with multiple reference under 35U.S.C . §102 set forth in the MPEP § 2131.01, part III).

As to claim 1: Hotta discloses in Fig. 1 an electronic device module comprising: a wiring substrate having an insulating substrate 1 with a porous structure (page 17, [0220], [0221], [0222]) including continuous pores (page 21, [0272]) and wiring conductors 4

within the pores (page 15, [0200]); and an electronic device directly connected to said wiring conductors formed in located within the pores (an electronic device, not show, but inherently is present as the structural feature of any type of the circuit boards (page 19, [0256])).*

* - APA discloses in Fig. 1 a semiconductor chip 1 directly connected to the wiring conductors formed in wiring substrate 2.

As to claim 2: Hotta discloses the electronic device module according to claim 1, wherein said wiring conductors in the wiring substrate 34, Fig. 3 are grouped into a first wiring conductor 33 extending in parallel with an electronic device mounting surface of the porous insulating substrate and a second wiring conductor 32 extending through the porous insulating substrate 34 from its top surface to bottom surface, Fig. 3.

As to claim 3: Hotta discloses the electronic device module according to claim 2, wherein said first wiring conductor 33, Fig. 3 is formed at a surface of said wiring substrate.

As to claim 4: Hotta discloses the electronic device module according to claim 2, wherein said first wiring conductor 33, Fig. 3 is embedded in said wiring substrate 34.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5.1. Claims 8-11 are rejected under 35U.S.C. 103(a) as being obvious over Hotta as applied to claim 1 above, and further in view of APA (in Background of the Invention section).

As to claims 8, 10 and 11: Hotta discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

except, Hotta doesn't explicitly discloses the electronic device is a semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted and wherein a size of the electronic device is smaller than the size of the wiring substrate and wherein the semiconductor chip is mounted on a top surface of the package base, with its terminal electrodes facing downwards, a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend to a bottom side of the package base.

APA teaches in Fig. 1 the electronic device is a semiconductor chip 1, and the wiring substrate 2 serves as a package base on which the semiconductor chip is mounted (Specification, page 1, lines 25-29) and wherein a size of the electronic device 1 is smaller than the size of the wiring substrate 2, Fig. 1 and wherein the semiconductor chip 1 is mounted on a top surface of the package base 2, with its terminal electrodes 4 facing downwards, a part of the wiring conductors of the package base are directly coupled to the semiconductor chip 1, and other part of the wiring conductors extend to a bottom side of the package base 2.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Hotta to include in his invention that the electronic device is a semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted and wherein a size of the electronic device is smaller than the size of the wiring substrate and wherein the semiconductor chip is mounted on a top surface of the package base, with its terminal electrodes facing downwards, a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend to a bottom side of the package base, motivated by its known suitability for its intended use. See MPEP §2144.07.

As to claim 9: Hotta discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

Although, Hotta doesn't explicitly discloses the insulating substrate has almost the same coefficient of thermal expansion as that of the electronic device, but Hotta teaches to use for the insulating material same material as is used in the application, namely "a photosensitive composition layer containing a compound forming an ion-exchange group upon irradiation with light" (Abstract). All of this materials are capable of performing the intended use (provide a value of a ratio (a/b) is about 4.5 or less) and then it meets the claim (claim 1). See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for Hotta to include in his invention the insulating substrate has almost the same coefficient of thermal expansion as that of the electronic device, motivated by its known suitability for its intended use. See MPEP §2144.07.

5.2. Claims 1-4, 6 and 8 are rejected under 35U.S.C. 103(a) as being obvious over of Okubora in view APA .

As to claim 1: Okubora discloses in Fig. 8F an electronic device module comprising: a wiring substrate 43, Fig. 8B having an insulating substrate (41, Fig. 8 and column 5, lines 18-22) and wiring conductors 43b, 44, Fig. 8F selectively formed in substrate; and an electronic device 50 directly connected to said wiring conductors substrate.

except , Okubora doesn't explicitly teach a substrate with a porous structure including continuous pores.

APA discloses at time the invention was made, it was well know to use a three-dimensional structure of the substrate including continuous pores (Specification, page 2, lines 1-9).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that a substrate with a porous structure including continuous pores as taught by APA because APA teaches that such structure would result in the benefit of stereoscopic wiring board with high degree of freedom in circuit design.

Instant modified Okubora clearly teaches all of the claimed limitations. Applicant amended claim 1 to introduce "wiring conductors selectively formed in the pores". However, this limitation is a process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Further, if the prior art structure ((Okubora as modified, disclosed insulating substrate with porous structure and wiring conductors) is capable of performing the intended use (connect an electronic device to electronic module), then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963).

As to claim 2: Okubora discloses the electronic device module according to claim 1, wherein said wiring conductors in the wiring substrate are grouped into a first wiring

conductor 43a, 43b extending in parallel with a electronic device mounting surface of the porous insulating substrate (41, Fig. 8 and column 5, lines 18-22) and a second wiring conductor 44 extending through the porous insulating substrate from its top surface to bottom surface, Fig. 8B. We consider through hole 44 as a second wiring conductor because as taught by Okubora via-holes which are metal plated at the inner wall to give a level of conductivity or filled with an electrically conductive paste for yielding the via holes to connect between the patterns in layers (column 8, lines 40-49).

As to claim 3: Okubora discloses the electronic device module according to claim 2, wherein said first wiring conductor 72 Fig. 9E is formed at a surface of said wiring substrate 71.

As to claim 4: Okubora discloses the electronic device module according to claim 2, wherein said first wiring conductor (71a, 71b Fig. 9A and column 8, lines 51-55) is embedded in said wiring substrate 71.

As to claim 6: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1, wherein the wiring substrate 49 and the electronic device 50 are directly connected with each other by bonding layers provided at contacts of the wiring conductors 44p with terminal electrodes 51 of the electronic device 50 Fig.8E.

As to claim 8: Okubora discloses the electronic device module according to claim 1, wherein a size of the electronic device 50 is smaller than the size of the wiring substrate 49, Fig.8E.

5.3. Claim 5 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view APA as applied to claims 1 and 2 above, and further in view of Shibasaki et al. (Patent #4296424) hereinafter Shibasaki.

As to claim 5: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 2, wherein, in a junction of the first 43a and second wiring conductors defined as planes in parallel with the electronic device 50 mounting surface of the wiring substrate, Fig. 8F,

except, Okubora doesn't explicitly teach the second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor.

Shibasaki discloses the second wiring conductor 3, 5a, 5b, Fig. 3 along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor. Shibasaki teaches (column 4, lines 27-41) the insulation substrate 1, Fig. 3, includes a photosensitive layer 2 that is, upon exposure to irradiated energy rays, exhibit conductive properties and forms electrodes. At time the invention was made, it was well know how to create conductors from photosensitive layer and that second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that the second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor to provide compound module.

5.4. Claim 7 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view APA as applied to claim 1 above, and further in view of Yasuda et al. (PGPub. # 2002/0100610) hereinafter Yasuda.

As to claim 7: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

except, Okubora doesn't explicitly teach a size of the electronic device and a size of the wiring substrate are substantially the same.

Yasuda discloses in Fig. 4A a size of the electronic device 5 and a size of the wiring substrate 6 are substantially the same. At time the invention was made, it was well know to use
so-called chip size package (CSP), when a size of the electronic device and a size of the wiring substrate are substantially the same.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention a size of the electronic device and a size of the wiring substrate are substantially the same.

Benefit of doing so is to reduce size of the semiconductor devices.

5.5. Claims 10 and 11 are rejected under 35U.S.C. 103(a) as being obvious over Okubora in view APA as applied to claim 1 above, and further in view of Japp et al. (Patent #6722031), hereinafter Japp.

As to claim 10: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

except, Okubora doesn't explicitly teach the electronic device is of semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted.

Japp discloses the electronic device is of semiconductor chip 160, Fig. 2, and the wiring substrate 1020 serves as a package base on which the semiconductor chip is mounted. At time the invention was made, it was well know to use the wiring substrate serves as a package base on which the semiconductor chip is mounted.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the electronic device is of semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted .

Benefit of doing so is to prevent damage of the chip and provide necessarily connections.

As to claim 11: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 10,

except, Okubora doesn't explicitly teach the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other
part of the wiring conductors extend to a bottom side of the package base.

Japp discloses in Fig. 2 the semiconductor chip 160 that is mounted on a top surface of the package base 1020, with its terminal electrodes 107 facing downwards, and a part of the wiring conductors 103 of the package base 1020 are directly coupled to the semiconductor chip 160, and other part of the wiring conductors 1006, 1008 extend to a bottom side of the package base. At time the invention was made, it was well know the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend to a bottom side of the package base.

Benefit of doing so is to provide connections of the chip with another printed circuit board.

5.6. Claim 12 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view APA and in view of Japp, as applied to claim 10 above, and further in view of Hur (Patent #6646334) hereinafter Hur.

As to claim 12: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 10,

except, Okubora doesn't explicitly teach the semiconductor chip that is mounted on a bottom surface of the package base, with its terminal electrodes facing upwards.

Hur teaches the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards. Therefore, at time the invention was made, it was well know the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards.

Benefit of doing so is to provide possibility to use both sides of the substrate.

Okubora also fail to discloses that a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Japp discloses in Fig. 2 the semiconductor chip 160 that is mounted on a surface of the package base 1020,and a part of the wiring conductors 103 of the package base 1020 are directly coupled to the semiconductor chip 160, and other part of the wiring conductors 1006, 1008 extend to a bottom side of the package base. At time the invention was made, it was well know that a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base, with its terminal electrodes facing upwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Benefit of doing so is to provide connections of the chip with another printed circuit board.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571)- 272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

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